

Fig. 1

Prior art

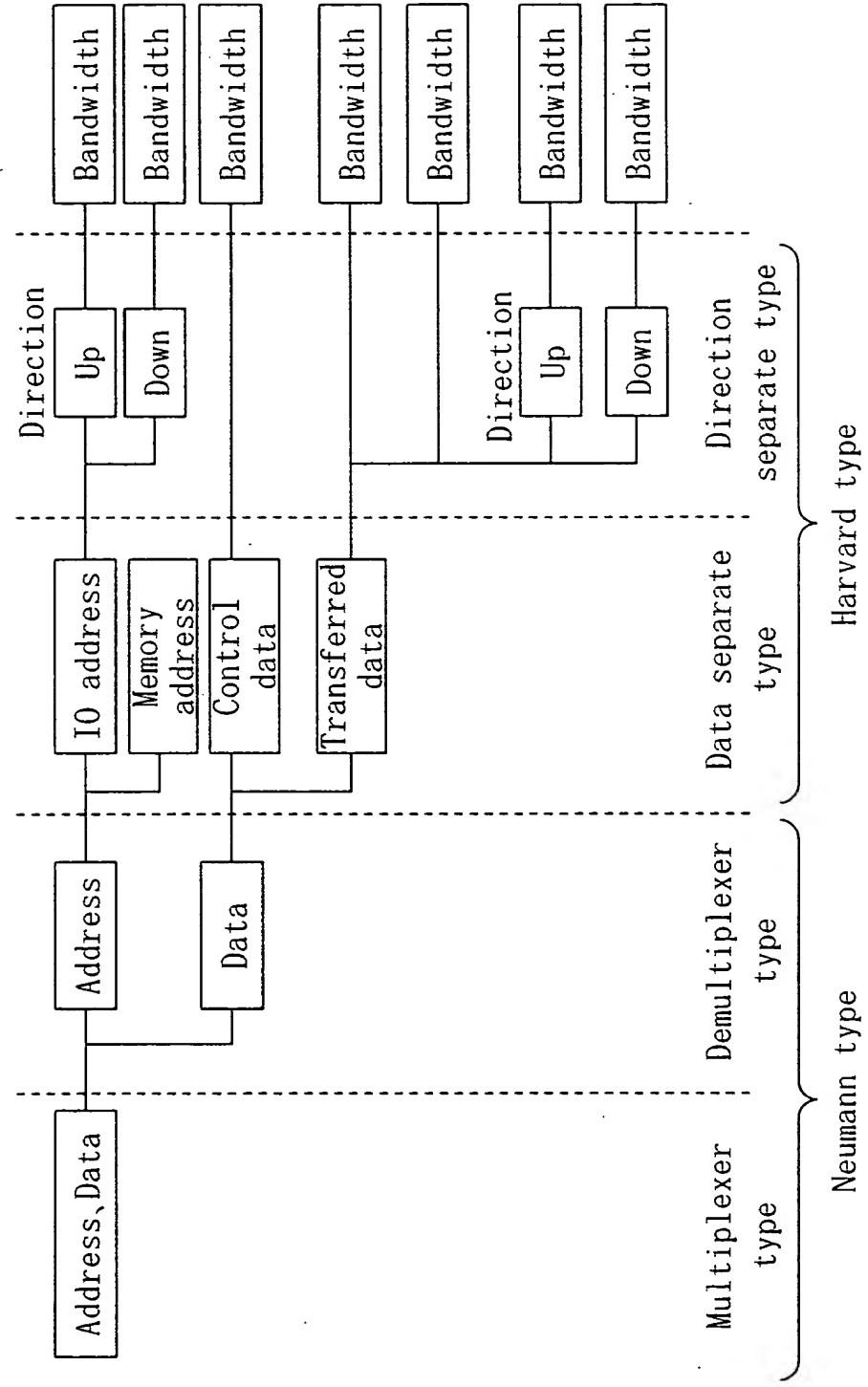


Fig. 2(a)

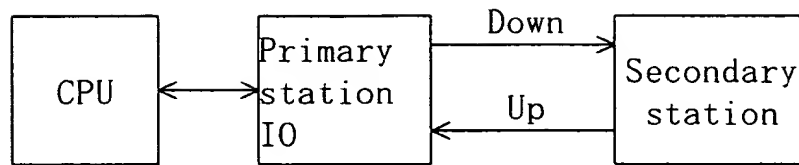


Fig. 2(b)

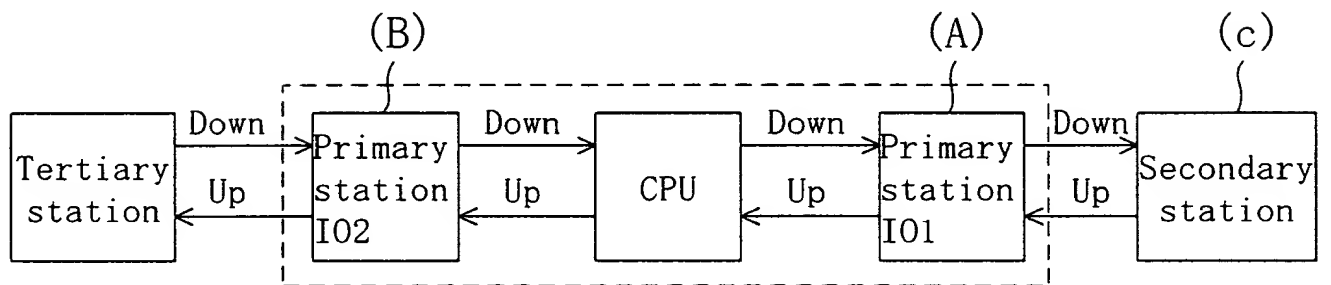


Fig. 2(c)

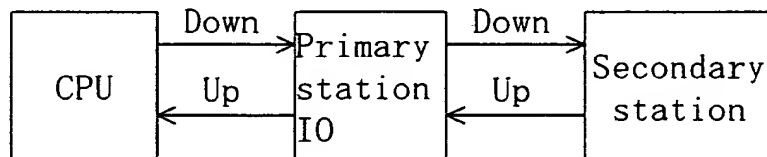


Fig. 3(a)

Multiplexer type

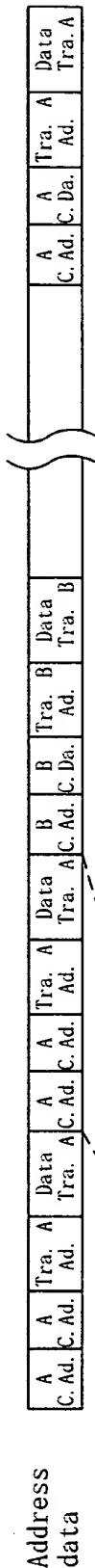


Fig. 3(b)

Demultiplexer type

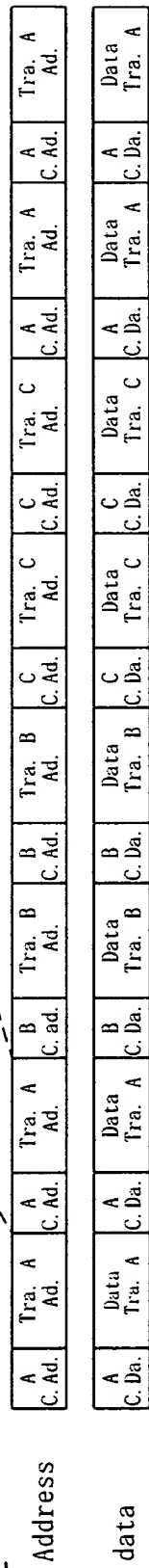


Fig. 3(c)

Data separate type

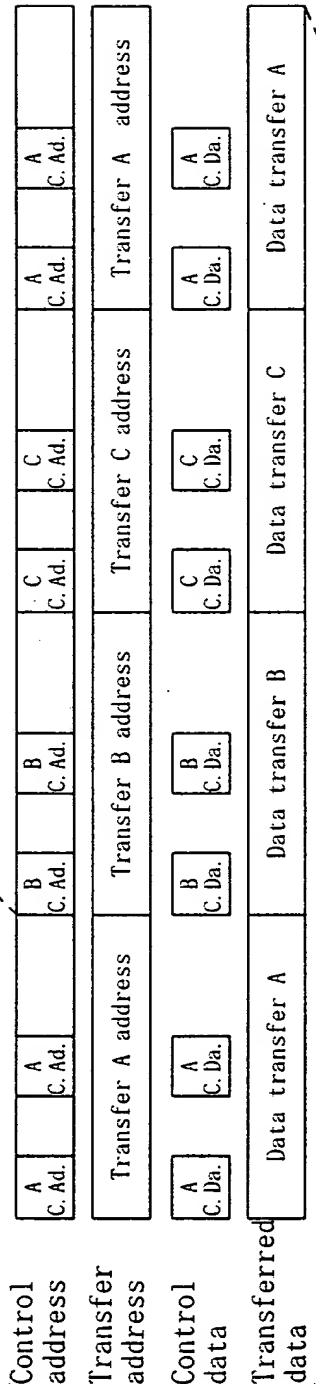


Fig. 3(d)

Direction separate type

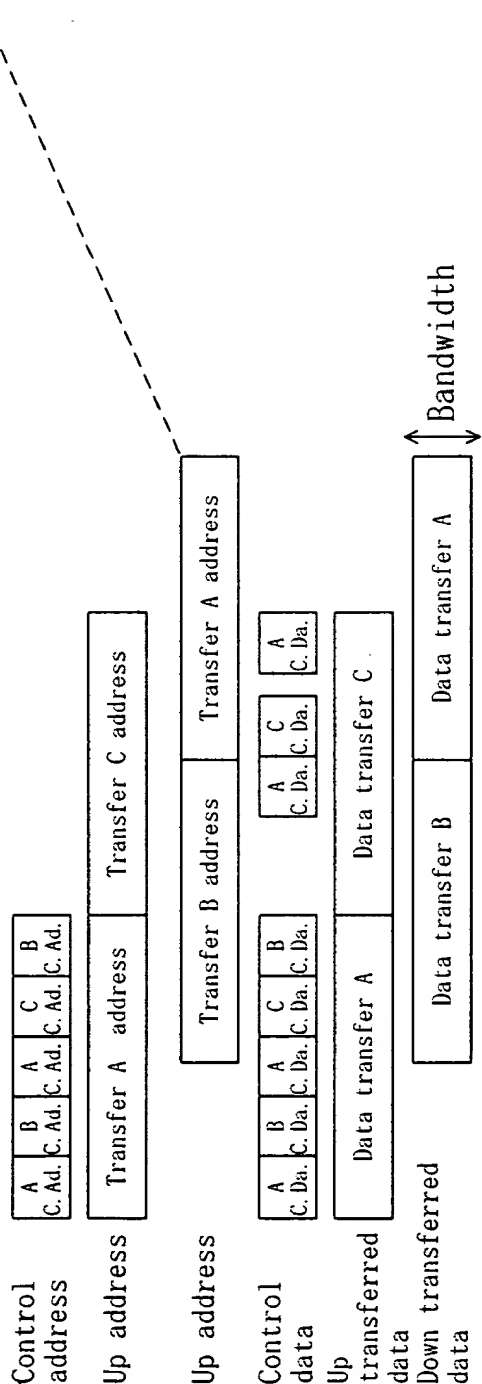
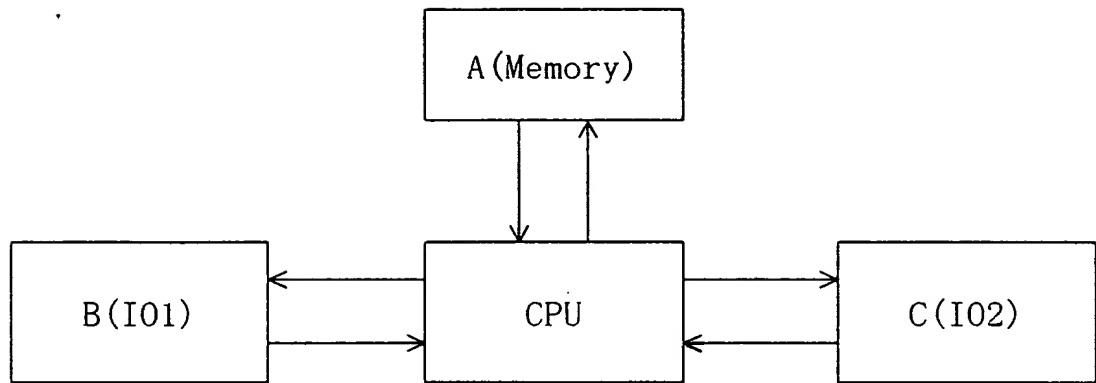
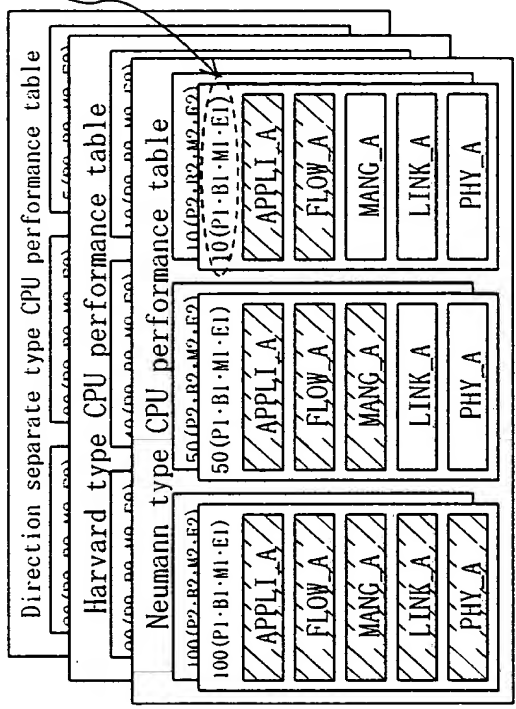


Fig. 4



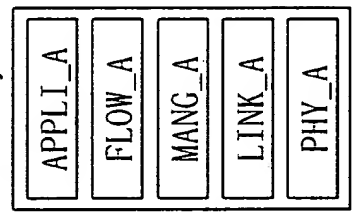
Performance index (throughput, bus width, instruction quantity, memory quantity)

Performance table



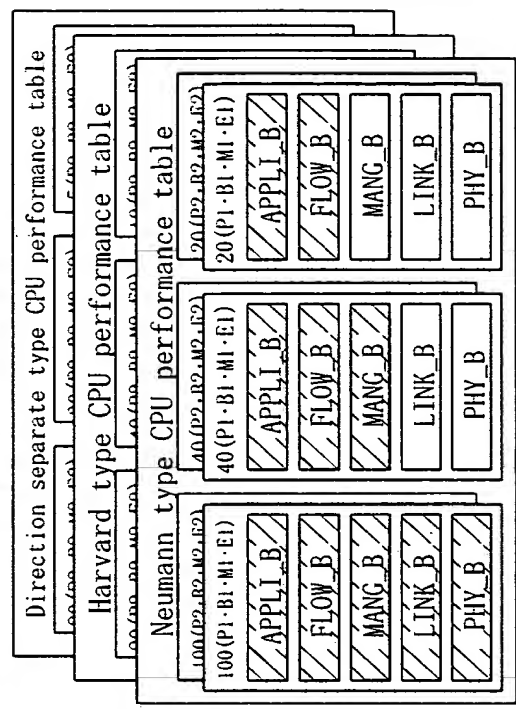
Operation model independent of OS and device

Library A



Specification model independent of OS and device

Fig. 5(a)



Library B

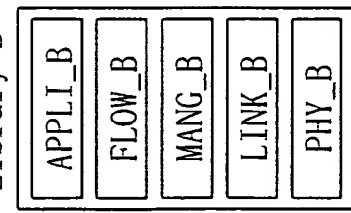


Fig. 5(b)

Fig. 6

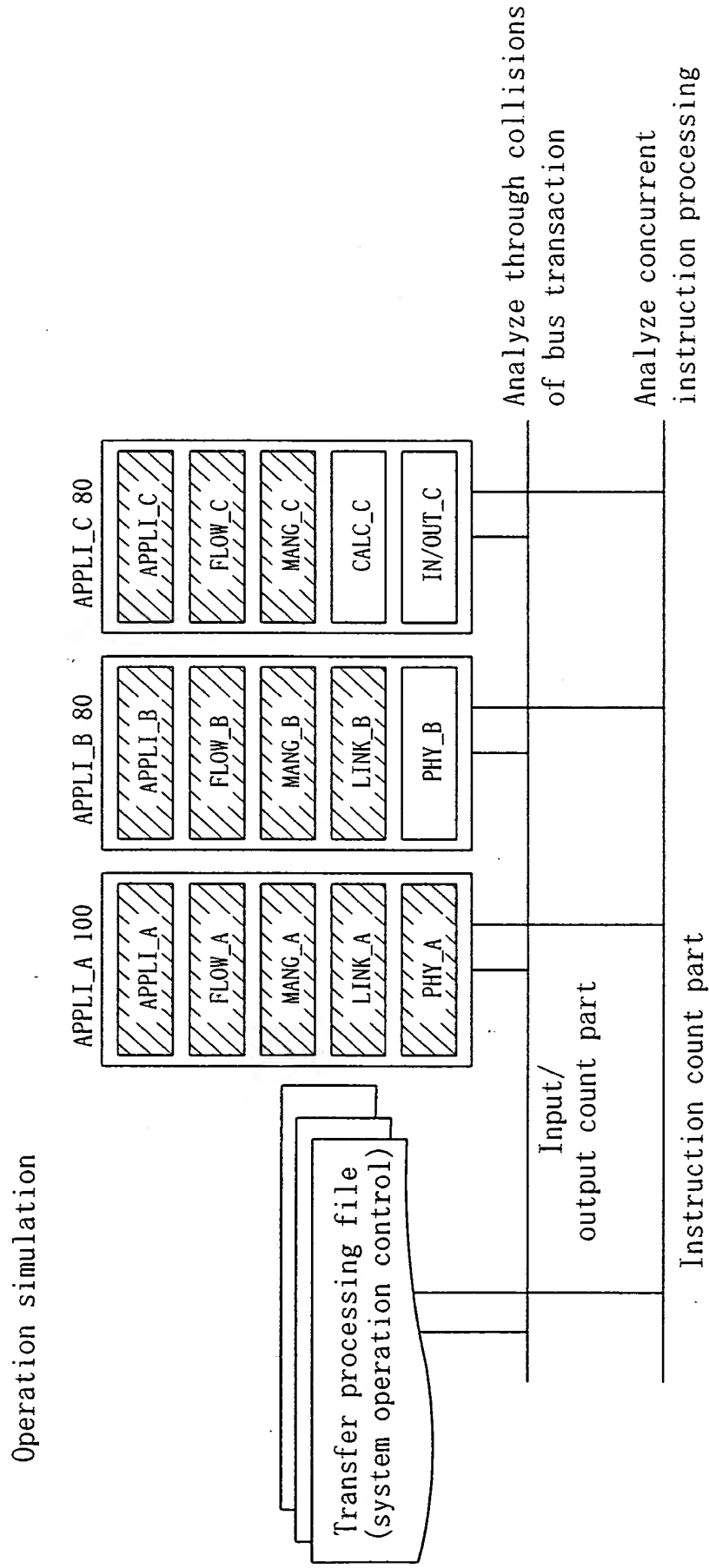


Fig. 7

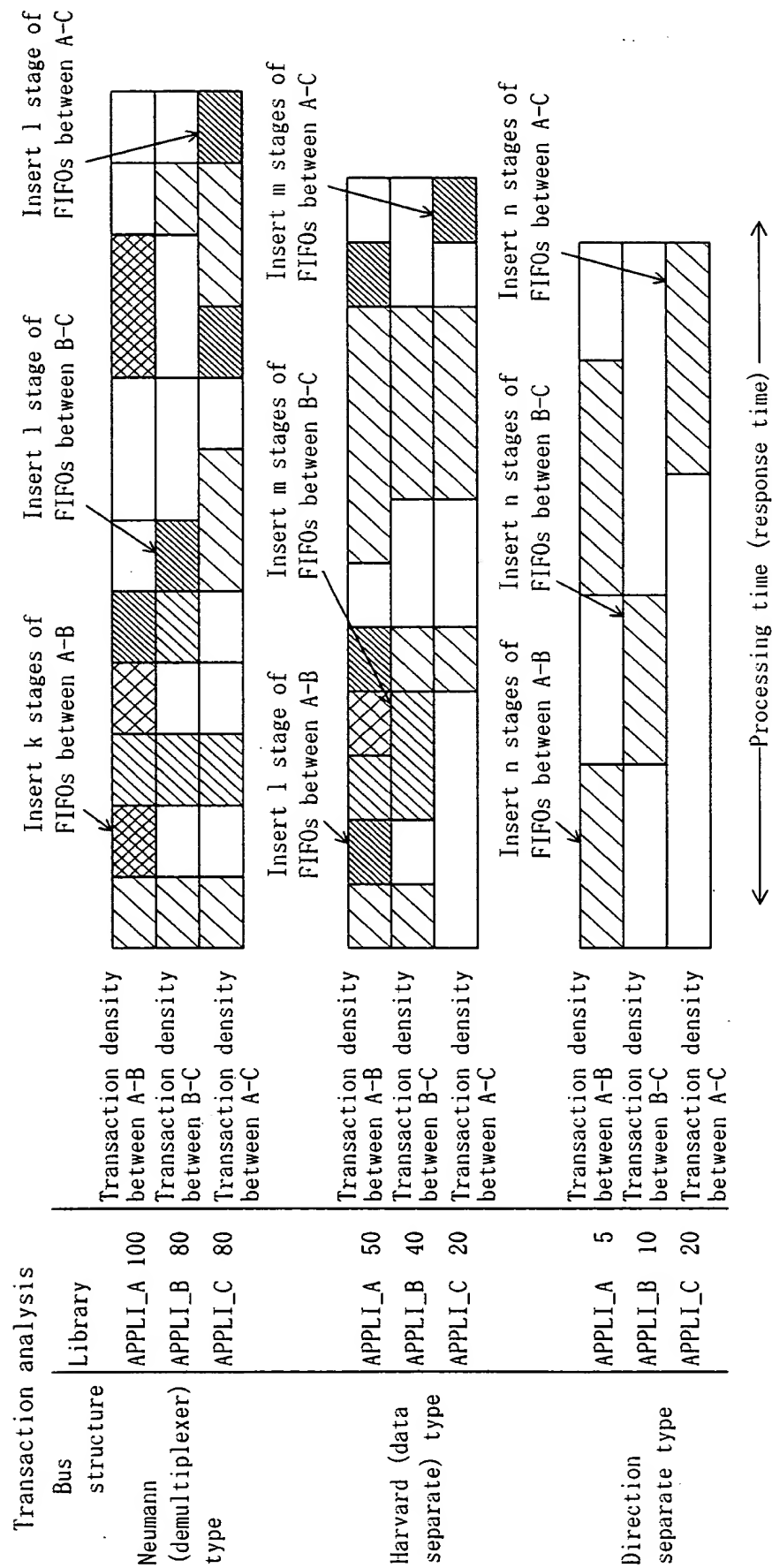


Fig. 8

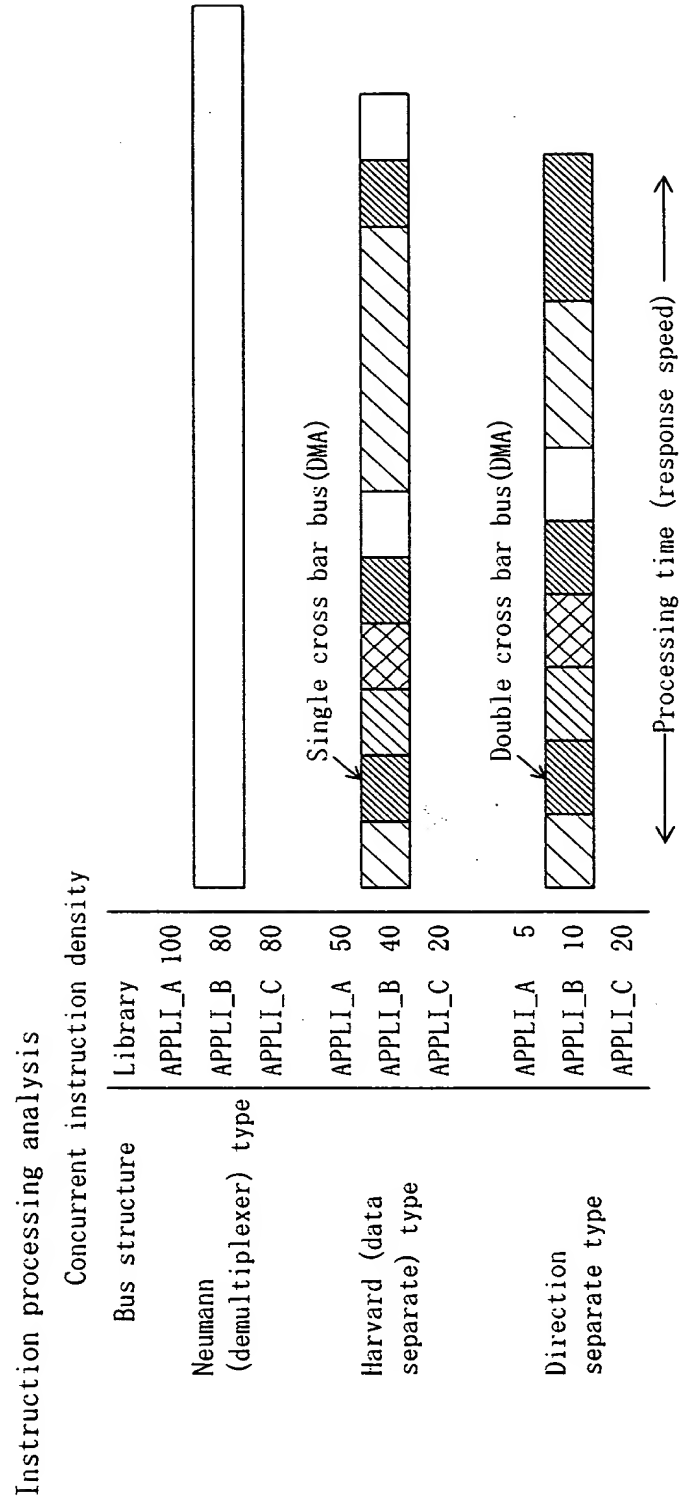


Fig. 9

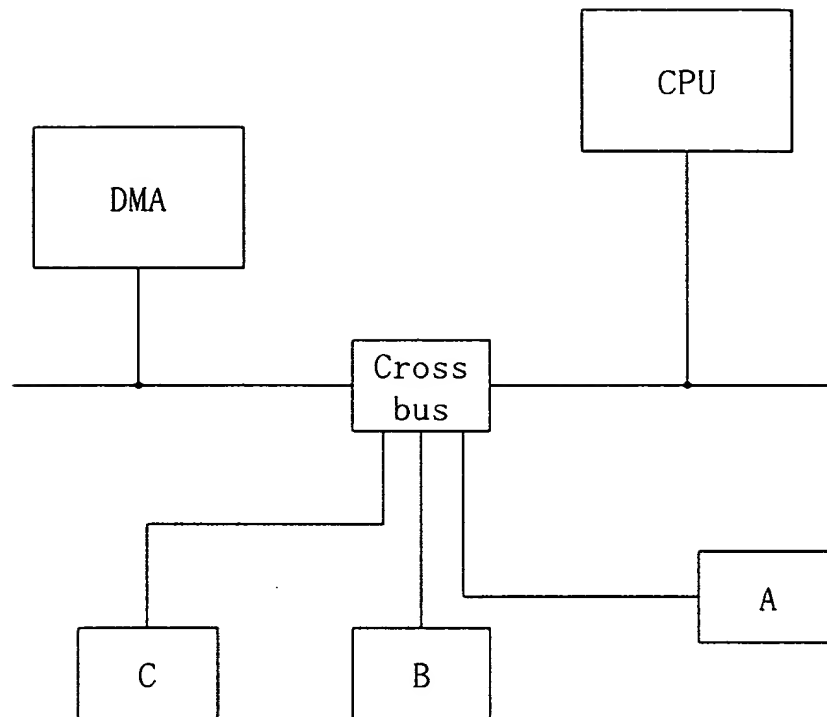


Fig. 10(a)

Performance
Bus transaction (T)

Response
time (R)

Processing quantity (E)

Fig. 10(b)

Power (maximum, average)

Processing quantity (E)

Concurrent active
ratio (A)

Hardware ratio (H)

Fig. 10(c)

Area (cost)

Bus width (B)

FIFO

quantity (F)

Memory quantity (M)

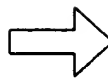


Fig. 10(d)

Performance

Analysis index

Area (cost)

Power

Analysis index (weighted index)

Fig. 11(a) Basis for determining performance index

Response time: R
Performance affecting coefficient of response time: lx
Bus transaction: T
Performance affecting coefficient of bus transaction: mx
Processing quantity: E
Performance affecting coefficient of processing quantity: nx
 $Rlx \times Tmx \times En = \text{Performance index: } x$
Example) lx = 1/1 sec., mx = 1/10 times, nx = 1/10 MIPS

Fig. 11(b) Basis for determining power index

Average (maximum) processing quantity: Eav (Emx)
Power affecting coefficient of processing quantity: ly
Hardware ratio: H
Power affecting coefficient of hardware ratio: my
Average (maximum) concurrent active ratio: Anv (Amx)
Power affecting coefficient of concurrent active ratio: ny
or $Eav ly \times Hmy \times Aavny = \text{Average power index} : y$
 $Emx ly \times Hmy \times Amxny = \text{Maximum power index}$
Example) ly = 1/10 MIPS, my = 1/20%, ny = 1/25%

Fig. 11(c) Basis for determining area index

Memory quantity: M
Area affecting coefficient of memory quantity: lz
FIFO quantity: F
Area affecting coefficient of FIFO quantity: mz
Bus width: B
Area affecting coefficient of bus width: nz
 $Mlz \times Fmz \times Bnz = \text{Area index: } z$
Example) lz = 1/1 kByte, mz = 1/128 bytes, nz = 1/16 bits

Fig. 11(d)

Basis for determining analysis index

Performance index (performance)
Coefficient affecting performance index: a
Power index (power)
Coefficient affecting power index: b
Area index (area)
Coefficient affecting area index: c
 $ax + by + cz = \text{Optimal index}$
Example) a=0.5, b=0.3, c=0.2

Fig. 12

Synthesis of optimal IF

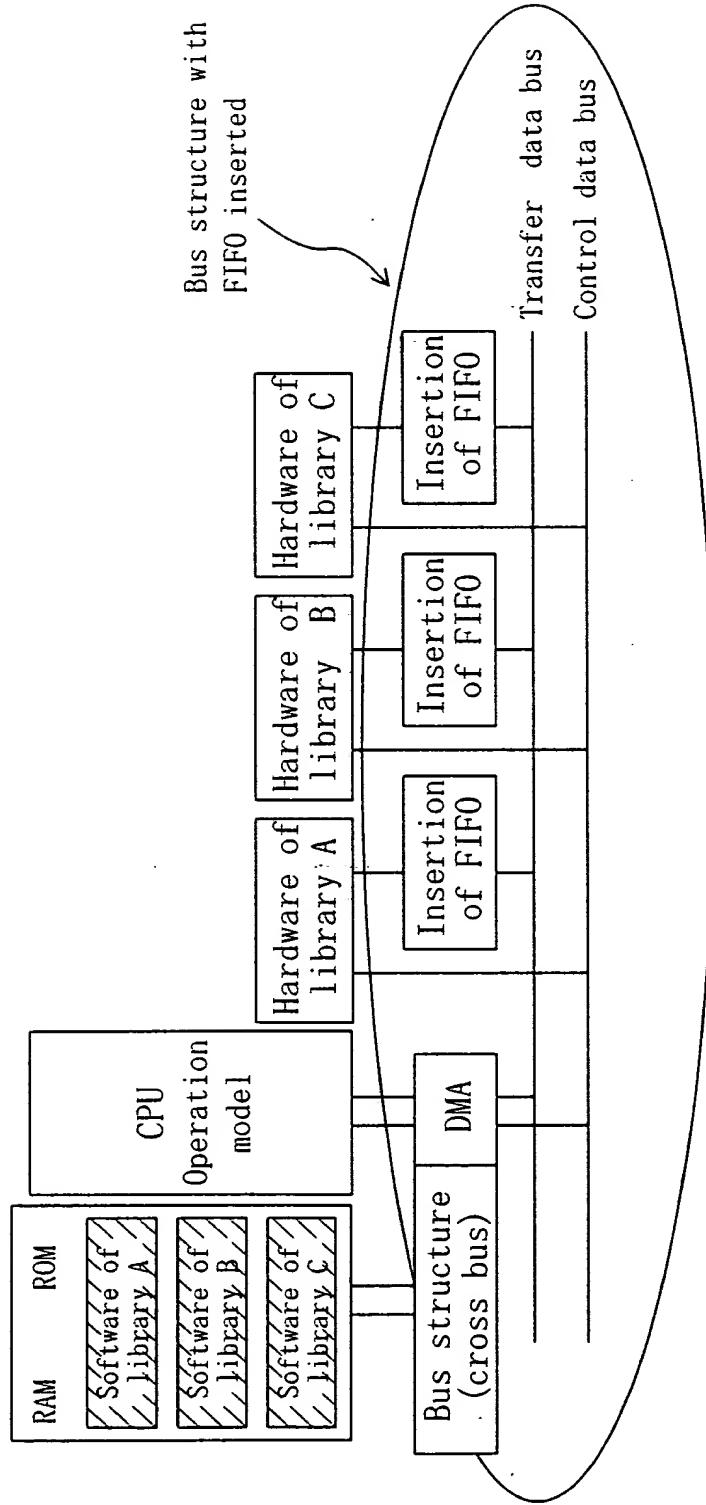


Fig. 13

